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FPGAs – CHRONOLOGICAL DEVELOPMENTS AND CHALLENGES

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ABSTRACT

The Field Programmable Gate Array (FPGA) industry is expanding both in market share and in innovation. The tailored FPGA features make them a better choice to include FPGA in an increasing number of applications in the upcoming years. A constant development of FPGA technology has led to minimize the gap of performance levels between FPGA and Application Specific Integrated Circuit (ASIC). Hence, in recent years, FPGA based platforms are proven more attractive than ASICs since their performance is high in addition to the low cost of the development process and short time to market. Therefore, nowadays, FPGA is highly attractive for a huge range of applications in communications, computing, avionics, security, automotive and consumer electronics. Field Programmable Gate Array industry has shown a steady growth with a market prediction value of USD 9 billion by 2023. Currently, the FPGA companies started growing in reserch areas such as Artifitial Intelligence (AI), Internet of Thing (IoT) and LIght Detection and Ranging (LIDAR).

The aim of this paper is to review the developments in FPGA.

Key words: FPGA, ASIC, PLD, Re-configurability, Re-programmability.

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1. INTRODUCTION

Until 1970, most digital logic designers were using standard digital components in designing digital electronics based products and systems. This concept of fixed-function devices were constrained due to Printed Circuit Board (PCB) scarcity as well as the product reliability due to the use of large number of interconnections. These drawbacks of the fixed-function devices have researched in the development of the need to design more compact digital circuits with

standard digital components without increasing design time and cost. This was the step that led to the development of Programmable Logic Devices (PLDs) [1], [2].

A PLD is an integrated circuit that is user-configurable and capable of implementing digital logic functions. In the 1970s, a new way of implementing digital logic functions using Programmable Read Only Memory (PROM), Erasable PROM (EPROM), and Electrically Erasable EEPROM were introduced as the earliest and simplest forms of PLDs. The PLD market growth has expanded very fast in so many directions in such a way that the semiconductor market accepted PLD a generic term [1], [2], [3].

At this stage, logic devices were classified into five general types as below.

- Standard Family Logic
- Custom and Fixed Function Logic
- PLDs
- Application Specific Integrated Circuit (ASICs)
- Microprocessors (MPUs) / Central Processing Units (CPUs)

Field Programmable Logic Device (FPLD) is another name coined for PLD. Programmable Logic Devices are usually classified into two categories, namely, Simple Programmable Logic Devices (SPDL) and High Capacity Programmable Logic Device (HCPLD). ROM, Programmable Logic Array (PLA), Programmable Array Logic (PAL) and Generic Array Logic (GAL) belong to the category of SPLD. Whereas, Complex Programmable Logic devices (CPLDs) and Field Programmable Gate Arrays (FPGAs) belong to the category of HCPLD [1], [4]. We present a visual depiction of summary of classification of digital logic IC designs in Fig. 1.

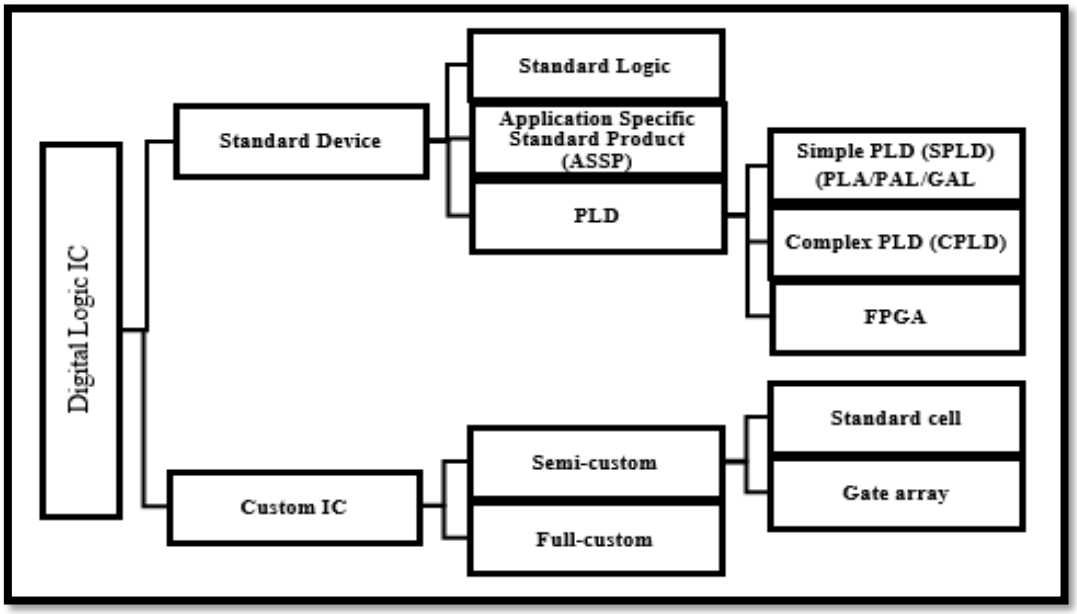

Figure 1 Classification: digital logic ICs

To integrate signals such as analogue signal, digital, mixed signals, ASICs are very useful. However, they are very costly and not friendly schedule. Using ASICs rather than FPGAs or CPLDs have many advantages and it depends on the design application. The advantages are represented in increasing both the performance and densities and the space requirements are decreased. The disadvantages are represented in the lacked of flexibility for changes and hard to debug test. For ASIC and PLDs technologies, some design applications that best suited for

both are there. More space is required for Logic designs that accomplished using FPGA. They have low performance, and therefore they require be migrated to an ASIC methodology. The process of the migration presents issues as the difference in the architecture and logic mapping to vendor specified functions [5] - [11].

There are various disadvantages associated with ASICs.

- High cost of prototyping increases the Non-Recurring Engineering (NRE) costs.
- In use of ASICs the risk of having multiple iterations are quite possible, which increases the cost and delays the project schedule.
- The ASIC designs usually have 50% probability of unsuccessful at the first trail to operate in the targeted.
- In the development cycle of an ASIC design process, it is difficult to make minor changes for refinements.
- In ASICs, testing and debugging processes are very difficult.
- In some situations, it might not suitable for ASIC technology to accommodate the design for integration of desired functions.
- The project of making the ASICs are extremely expensive in terms of cost and time.

However, the increased production volume reduces the overall cost of the design per unit. But the volume of the design may not reach the break-even point to be cost effective compared to the use of standard components as can be seen in Fig. 2.

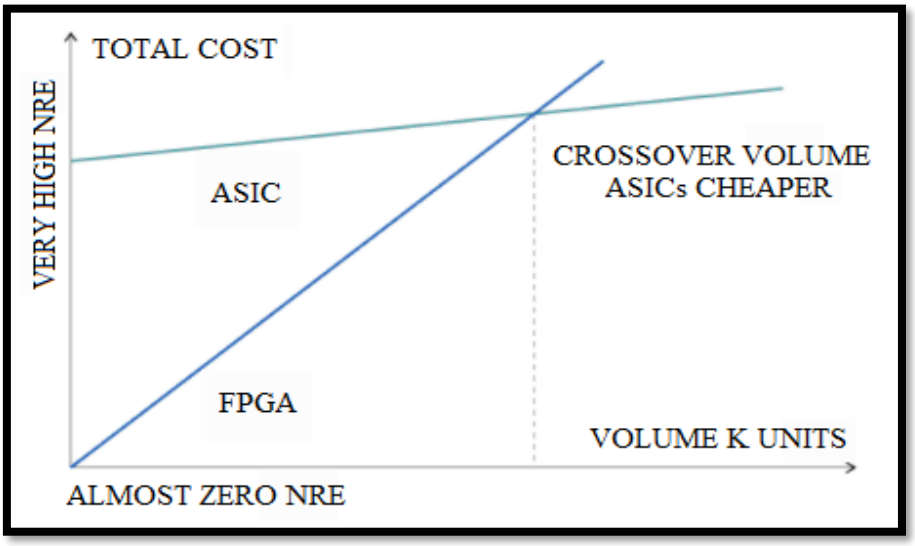

Figure 2 ASIC and FPGA cost analysis

During the period of 1985-1990, the ASIC industry was unstable due to emergence of new companies' products and methodologies based on other technologies. The volatile situation of ASIC industry can be judged with a predicted projection of the industry in mid of 1980s; the prediction was that ASIC designs would be taking over 50% of the electronic design market by 1990. However, what observed in 1990 that the ASIC market turned out to be approximately only 10% [12] - [14].

In 1983, British application engineers, Rodney Smith with Robert Hartmann, James Sansbury, and Paul Newhagen established the Altera Corporation with a seed money of USD 500,000. By 1984, Alera started marketing the "alterable" chips as their first-generation products. By 1988, Altera's went public with asset of value of USD 38 million. Then, Altera

introduced a new generation of chip, “the first Erasable Programmable Logic Device (EPLD) [15].

In 1989, the first integrated graphical design environment that put together design simulation, compilation, schematic input, and programming software all in one platform was introduced by the Altera company. The Altera continued to break new barriers by introducing their first FPGA in 1992. By the mid of 1990s, Altera became as one of the challenging competitors of the Xilinx company. However, Intel acquired Altera for USD 16.8 billion on December 28, 2015 with condition of keeping the Altera name for their product line. At this point of time, Xilinx had about 50% market share while Altera (Intel) has about 37% and Lattice Semiconductor has about 13% market share. In October 2020, AMD has acquired Xilinx. By this way, the two largest CPU vendors have acquired the two largest FPGA companies. Since more than 20 years, FPGA industry (see Table 1) has shown a steady growth with a market prediction value of USD 9 billion by 2023. Currently, the FPGA companies started growing in market areas such as: Artificial Intelligence (AI), Internet of Thing (IoT) and Light Detection and Ranging (LIDAR) [16] - [22].

Table 1 The performance of ...

Variable	Website
Xilinx (AMD) Altera (Intel) Lattice Semiconductor QuickLogic Microchip Technology	www.xilinx.com www.altera.com www.latticesemi.com www.quicklogic.com www.microchip.com
Achronix	www.achronix.com
Efinix	www.efinixinc.com

2. FPGAs – WITH EDGE OVER AND CONSTRAINTS

Field-Programmable Gate Arrays provide a number of advantages over ASIC technologies such as standard cells. FPGAs can often be reconfigured if an error is experienced. The time and cost involved in reconfiguration are fractions of seconds and a few dollars respectively.

FPGAs have the flexibility of having their functionality changed through reprogramming comes at a significant cost in area, delay, and power consumption. More space area for FPGA is required when compared with ASIC standard cell, approximately 20 to 35 times more. However, the performance in terms of the speed roughly is 3 to 4 times slower than an ASIC and much dynamic power are consumed, roughly 10 times. These disadvantages arise largely from an FPGA’s programmable routing fabric that trades area, speed, and power in return for instant fabrication. Despite these disadvantages, FPGAs offer an alternative way to implement the digital system because the volume cost is low and turnaround time is fast.

The computational power is considered as the most appealing aspect of FPGAs. As an example, the typical signal-processing FPGA can have anywhere from 1000 to 44,000 slices. Two lookup tables, two flip-flops, logic cells, and memory are required for each slice. 3000 slices or less than 50 percent of the FPGA's capabilities are required to implement 802.11a, a communications standard that is beyond the abilities of any traditional Digital Signal Processing (DSP). This is turn shows that the importance of a high degree of parallelism in the use of many accumulators for complex waveform signal processes implementation in parallel.

From a performance prospect, consuming a significant amount of power is the most FPGA significant drawback, which causes it less practical for battery-powered handheld subscriber solutions. For example, an FPGA with about 9000 slices mentioned before is rated at slightly

over 2 W of power expenditure, whereas a low-power DSP for handheld use is rated at 65 to 160 m W, depending on clock speed.

Thus, it can be concluded that in particularly with challenging constraints and in general with edge over opportunities. Nowadays, FPGAs are becoming increasingly important in many digital systems due to their high performance and flexibility. As a result of part of our study related to edge over comparison of between FPGA and ASIC, we present a summary through Table 2.

Table 2 The edge over comparative study between FPGA and ASIC

Attributes	FPGA	ASIC
NRE	+	-
Performance	-	+
Time to market	+	-
Design flow	+	-
Cost per function (high volume)	-	+
Barrier to entry	+	-
Energy efficient	-	+
Analog blocks	-	+

3. AN OVERVIEW OF BASIC FPGA ARCHITECTURE

As illustrated in Fig. 3, traditionally, a basic FPGA architecture consists of three main resources. The resources are as listed below:

- Configurable Logic Blocks (CLBs)
- Programmable routing switches
- I/O blocks

A CLB typically contains a small amount of logic gates, memory and multiplier blocks that can be configured to perform Boolean operations on the inputs to the CLB block. A small memory can be used to construct the logic because it is considered as a lookup table. This is referred as a LUT. The CLBs are surrounded by a system of programmable interconnects, called a fabric, that routes signals between CLBs. The array is surrounded by programmable input/output blocks (Pads), labeled I/O in the figure that connect the chip to the outside world. In addition, Switch Matrix/ Interconnection Wires block exists there.

The logic cell in the CLB block is connected to a small number of flip-flops in the CLB block itself. The CLBs are also connected to switch matrices that in turn are connected to each other using a network of wires. A schematic diagram of a traditional FPGA is shown in Fig. 4.

A large number of logic cells is contained in An FPGA. To implement a certain set of functions, each logic cell can be configured. A fixed number of inputs and outputs are there in each logic cell. The types of logic cells used in FPGAs are of types as:

- Multiplexer based logic cells
- Memory based logic cells

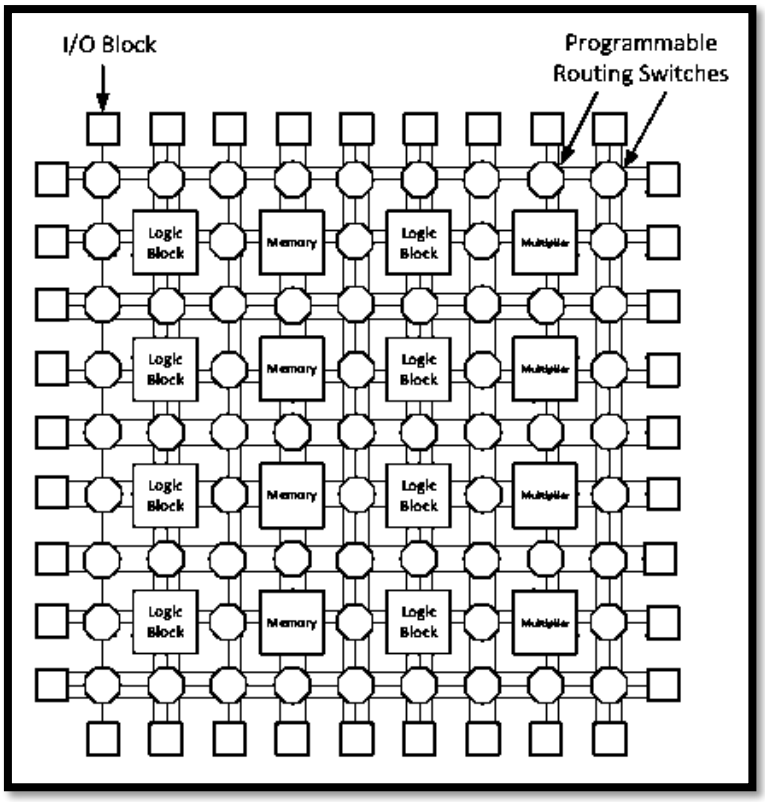

Figure 3. The generic structure of the FPGA – A basic architecture model

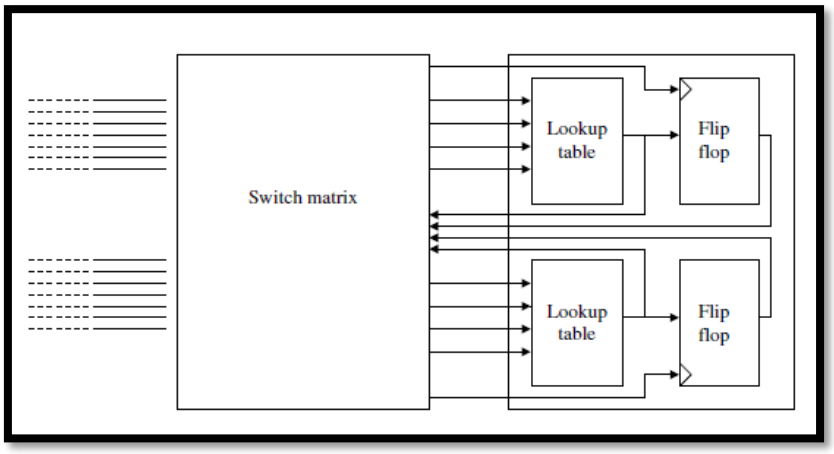

Figure 4. The fabric of CLB and switch matrix

4. MEMORY BASED FPGAS - LUT BASED CLB

A memory based logic cell is also called LUT based logic cell, where memory is the LUT. K-input LUT (memory) can implement any function of up to K variables. D flip-flops can be included in LUT based logic cells to implement sequential circuits (see Fig. 5). A set of 1-bit storage elements is used in LUT to implement the logic functions. K-input can implement 22K different logic functions as depicted in Fig. 6. The logic in LUT can be easily changed by changing the bits stored in the SRAM cells. To make it more readable, we present an implementation of 2-input LUT as Example 1 below.

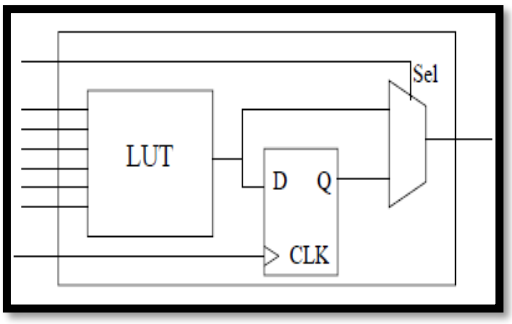

Figure 5. LUT based logic cells to implement sequential circuits

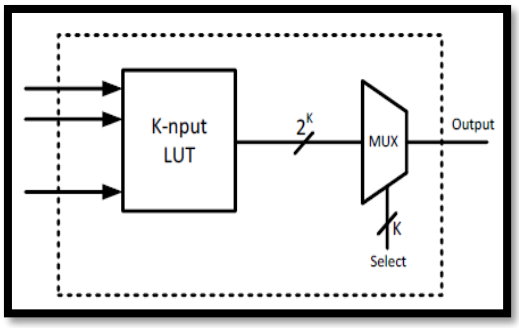

Figure 6. A K-input LUT

Example 1

Let us consider to realize a 2-input (X1, X2) Excusive - NOR function (f(X1, X2)). The Boolean function f(X1, X2) can be expressed as f(X1, X2) = ∑m0, m3. The implementation of the function using 2-input LUT is shown in Fig. 7.

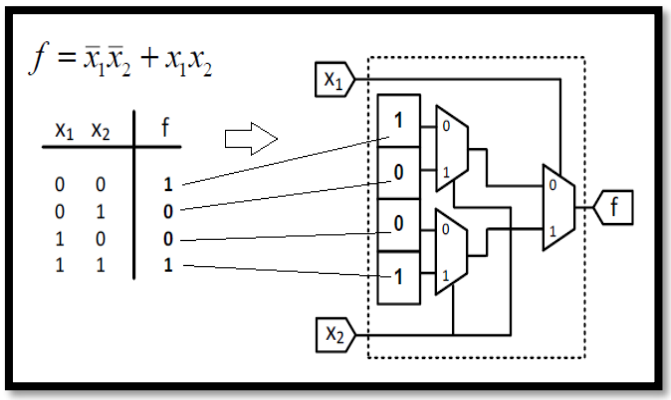

Figure 7. A 2-input LUT (Example 1)

The CLB in anti-fuse-based FPGAs are generally based on multiplexing. Therefore, Boolean functions can be realized using MUXs based on Shannon's expansion. MUX-Based CLB (can also be used to build latches/registers). Shown in Fig. 8 to 10 are some examples of MUX-Based configurable logic blocks.

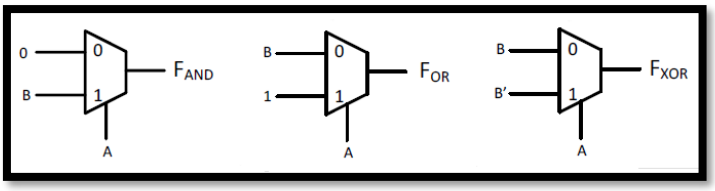

Figure 8. Examples of MUX based CLB realizing OR, AND, and XOR gates

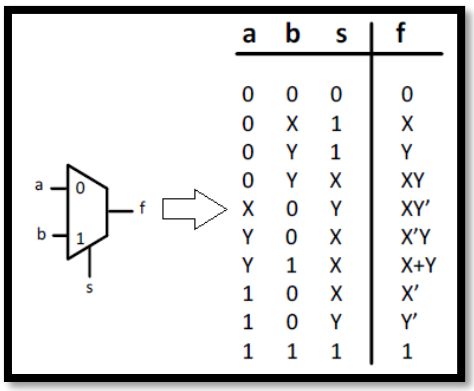

Figure 9. A MUX based CLB realizing various Boolean functions

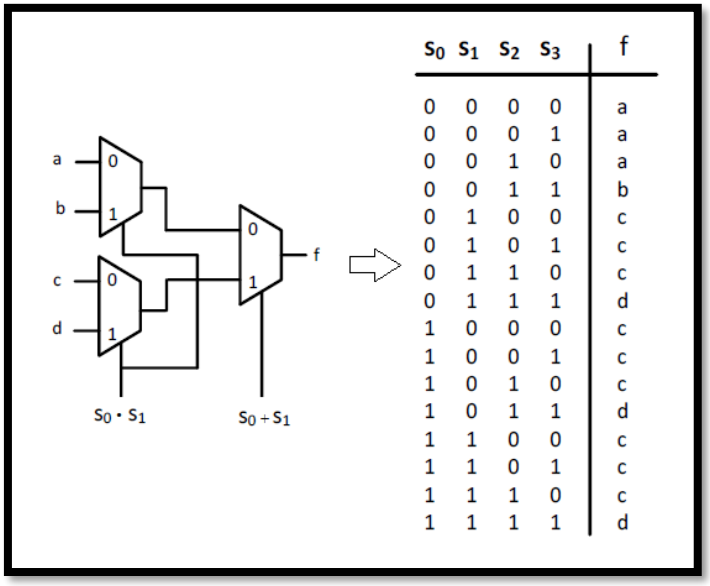

Figure 10. Example of MUX based CLB with complex select lines

5. FPGAs – IN MODERN ERA MEMORY BASED FPGAS - LUT BASED CLB

Xilinx (AMD)

Xilinx was co-founded in 1984 by Ross Freeman, who was the inventor of FPGA [23]. Since then, Xilinx took the lead in the industry of FPGAs worldwide. However, on 27 October 2020, AMD Company announced that it has acquired Xilinx [24], [25].

Xilinx in 1984 introduced the first modern-era FPGA that contained the now classic array of CLBs. They contained 64 logic blocks and 58 inputs and outputs. 330 K equivalent logic blocks and around 1100 inputs and outputs are now contained in the modern FPGAs [26].

Xilinx provides to its customer with a line of products that include programmable devices, software design tools, and Intellectual Property (IP) hardware functions.

When it comes to reconfigurable computing devices, Xilinx offers several options. These options vary in their technology node (i.e., 16nm, 20, nm, 28, nm, or 45nm) and capability (i.e., speed vs. power consumption) [27]. For instance, if we consider the latest technology node, Xilinx offers 3 devices that were fabricated using 16nm transistor feature size; namely, Artix UltraScale+, Kintex UltraScale+, and Virtex UltraScale+. Artix UltraScale+ provides a low-power, low-cost solution. Alternatively, Virtex UltraScale+ represents the other end of the extreme, where it provides the highest capacity and performance. On the other hand, the Kintex UltraScale+ can be perceived as the middle ground between Artix and Virtex.

In particular, the Virtex UltraScale+ [28] is a 3D IC, which integrates PCIs blocks, Digital Signal Processing (DSP) cores, on-chip memory, and high-speed transceivers. In terms of programmable fabric, the Virtex devices embed 862 – 3,780 thousand logic cells, depending on which specific device is selected from the family of Virtex UltraScale+. Furthermore, there is between 115.3 – 455 Mb on-chip memory and 2,280 – 12,288 DSP cells.

Virtex UltraScale+ is ideal to use in data centers for accelerating complex workloads. In addition, the high speed and low latency offered by such devices make them suitable for integration with 5G telecommunication infrastructure. Additionally, other complex tasks such as machine vision and robotics can take avail of reconfigurable computing devices.

Altera (Intel)

The British applications engineer, Rodney Smith. Founded it and by using a $500,000 as seed money. On December 28th, 2015, Intel acquired Altera for $16.8 billion, putting an end to the independently-run company, although the Altera name is still used for their product line [29] – [31].

The Altera Company that creates FPGA and PLDs along with development software. Some products are produced by Altera are:

- FPGAs: Arria, Cyclone, and Stratix
- CPLDs: Max Series
- Enpirion Power SoC DC-DC Power Solutions
- Quartus II Design Software

The Altera development was urged by the industry and because of the manufacturing process, the need for programmable chips became a necessity to which often required revision when making specific customized chips. Intel quickly marketed the programmable chips created by Altera and soon the fortunes of Altera took off. By 1988, Altera's sales reached $38 million and the company went public. As Altera expanded, they introduced a new generation of their chip design and created the first erasable PLD (EPLD). This innovation allowed their vendors to save board space and time in programming the chips [29] – [31].

In 1989, first integrated graphical design environment is produced where the design simulation, compilation, schematic input, and programming software all are added together in one place. This helps to invigorate the industry and put Altera at the top of its field. New barriers are broken by the company by introducing their first FPGA in 1992. The flexible logic elements are used in the contrary of the standard structured ones, Altera was going up by the mid of 1990s against Xilinx, their major competitor, in creating hardware products that each rival managed to top in terms of performance. The Mega functions Partners Program Altera is created that brought in several companies for supporting with some of the products offered by the

company. Synopsis is an example of the companies, where an agreement of five-year achieved the development of a new line of CPLDs [29] – [31].

Today, Intel® Agilex™ FPGA devices leverage heterogeneous 3D system-in-package (SiP) technology to integrate Intel's first FPGA fabric built on 10nm SuperFin Technology and 2nd Gen Intel® Hyperflex™ FPGA Architecture to deliver up to 45% higher performance (geomean vs. Intel® Stratix® 10) or up to 40% lower power1 for applications in data center, networking, and edge compute. When compared to our competition's 7nm FPGA portfolio, Intel® Agilex™ delivers ~2X better fabric performance per watt.1 Intel® Agilex™ SoC FPGA devices also integrate the quad-core Arm* Cortex-A 53 processor to provide high system integration [32].

Intel® Agilex™ F-Series 027FPGA (R24C), launched in 2019, contains 2692760 Logic Elements (LE), 8528 DSP blocks and has provision of maximum embedded memory as 8528 Mb. These FPGAs with advanced DSP capabilities are optimized for applications in Data Center, Networking, and Edge Computing [33].

Intel® Agilex™ I-Series SoC FPGA devices are optimized for applications, which are bandwidth intensive and require high performance processor interfaces [32].

The Intel product, which is channel and as announced that it is coming soon is - Intel® Agilex™ M-Series SoC FPGAs optimized for computing and memory intensive applications. With Coherent attach to Intel® Xeon® processors, HBM integration, hardened DDR5 controller, and Intel® Optane™ DC persistent memory support the Intel® Agilex™ M-Series SoC FPGAs are optimized for data-intensive applications, which need massive memory in addition to high bandwidth channels [29] – [33].

6. CONCLUSION

Since the introduction of Field-programmable gate arrays thirty five years ago, the industry have evolved, giving way to new generations of FPGAs that can be used in a broader range of applications. In the past, FPGAs were selected for lower speed and lower volume designs, but as the scope of FPGAs started to shift to wider range of applications, the industry evolved producing FPGAs successfully, with better logic density and performance [34] – [36].

Due to the advantages of re-configurability, re-programmability and fast time-to-market concept with no up-front NRE, modern FPGAs became reliable devices. Based on the rapid prototype capabilities of FPGAs, the logic can be rapidly conducted and verified in hardware, while in field-reconfiguration can keep up with future modifications without modifying the board layout. The Intel and AMD products are continued growing and provide a synchronized interfaces with technological developments.

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